Remarks

Thorough examination by the Examiner is noted and appreciated.

The listing of the claims now serves to cancel claims 1-21 since still listed as pending in the Application.

Claim Rejections under 35 USC 103

1. Claims 22-26, 28, 29, and 39 to 42 stand rejected under 35 USC 103(a) as being unpatentable over Parker et al. (US 6,787,440).

Parker et al. disclose a method for making a semiconductor device where a **buffer layer is formed between a substrate and a high-K dielectric layer** (see Abstract). The buffer layer is taught to be formed for the purpose of **avoiding shorting through a thin gate dielectric** (col 1, lines 35-36). In addition Parker et al. teach reoxidizing (e.g., col 3, lines 11-15) the high-K

dielectric layer **following formation of the high-K dielectric on the buffer layer** to improve an interface between the high-K dielectric and the gate electrode (col 1, lines 38-40; col 2, lines 21-30). A gate electrode is formed **on** the high-K dielectric following the reoxidation process (col 3, lines 66-67). In another embodiment the high-K dielectric layer is formed directly on the substrate and the buffer layer formed **between the high-K dielectric and the substrate** (col 4, lines 16-21) **during reoxidation** of the high-K dielectric layer (col 4, lines 38-46). Parker et al. disclose that the buffer layer is formed of silicon dioxide or silicon oxynitride ((col 2, lines 35-39).

Thus, Parker et al. disclose an **entirely different structure** than Applicants disclosed and claimed invention. Parker et al. do not disclose several aspects of Applicants disclosed and claimed invention including:

"**a buffer dielectric layer on the high-K gate dielectric layer**, the buffer dielectric layer comprising dopants selected from the group consisting of a metal, a semiconductor, and

nitrogen; and,

a gate electrode layer **on** the buffer dielectric layer."

Parker et al. is clearly insufficient to make out a *prima facie* case of obviousness with respect to Applicants disclosed and claimed invention.

Examiner misunderstands Applicants invention as the claimed material and asserts that Applicants has not pointed out how the claimed materials distinguish over Parker et al.

The structure of Parker et al. (i.e., substrate/buffer layer/high-K dielectric layer/gate electrode layer) **presents the very problem that Applicants disclosed and claimed invention overcomes:** "A gate structure with a reduced Voltage threshold (V_{th}) shift". To reiterate, Parker et al. do not show or suggest Applicants structure including (**high-K dielectric layer/buffer layer/ gate electrode layer**).

Applicants discuss the problem of the structure of Parker

et al. in the prior art at paragraphs 004 and 005:

"There have been, however, difficulties in forming high k gate dielectrics to achieve acceptable threshold Voltage behavior in CMOS devices. Frequently, a relatively large shift in flatband Voltage or equivalent threshold Voltage occurs when high K dielectrics are used in a gate dielectric stack for both NMOS and PMOS devices. For example, hafnium oxide (e.g., HfO_2) when used in the gate dielectric stack exhibits a shift of from about 300 mV in NMOS devices and about 700 mV in PMOS devices compared to conventional SiO_2 gate dielectrics.

The presence of undesirable interfacial states and diffusion of metals into the high-K dielectric is believed to contribute to flatband and threshold Voltage shifts. Several approaches, from treating the base oxide layer, to post deposition annealing of the high-K dielectric prior to methods of polysilicon electrode layer deposition have been proposed. Proposed approaches so far have met with limited success, threshold Voltages still exhibiting larges differences (shifts) compared to expected electrical performance. As a result, the integration of high-K gate dielectric gates in gate structures with acceptable electrical behavior including acceptable threshold Voltage behavior in low power CMOS devices remains a problem to be overcome."

In addition, Parker et al. nowhere recognizes the problem that Applicants have recognized and solved by their disclosed

and claimed invention.

Applicants have also clearly pointed out the benefits of their invention see e.g. paragraph 0030:

Thus, a gate structure and method for forming the same has been presented to improve an electrical performance of a high-K gate dielectric. For example, the buffer layer formed on the top portion of the high-K gate dielectric according to preferred embodiments accomplishes several beneficial functions including avoiding Fermi-level pinning at a high-K gate/gate electrode interface, for example caused by the formation of interface metal-Si bonds. The buffer layer is preferably doped with a dopant type and level to reduce a Voltage threshold (V_{th}) shift compared to the absence of the buffer layer. Preferably, the buffer dielectric layer dopant type and dopant level reduces Voltage threshold (V_{th}) shift less than about half of the forbidden energy bandgap (Eg) at the gate electrode/doped buffer dielectric interface. For example, in an exemplary implementation, silicon (polysilicon) has a forbidden energy bandgap (E_g) of about 1.12 eV, where the buffer layer reduces the Voltage threshold shift to less than half that amount (e.g., E_g), even more preferably less than about one quarter of that amount.

Since the cited art **fails to show or suggest the structure of Applicants**, the issue of dopant materials, or buffer layer

materials, used in Applicants structure is not relevant to obviousness since Applicants structure is not disclosed or suggested, and any argument of routine optimization is misplaced

Since Examiner has failed to make out a *prima facie* case of obviousness with respect to Applicants independent claims, neither has one been made out with respect to dependent claims.

Examiner further argues that the inclusion of an interfacial layer in claims 25, 26 and 41 is obvious "because it corresponds to the buffer layer being below the high-K dielectric" (in Parker et al.). Applicants respectfully suggest Examiner is ignoring Applicants disclosed and claimed structure of the buffer layer between the high-K dielectric and the gate electrode; the presence of an interfacial layer **in the absence of Applicants structure in the prior art** does not help Examiner is reproducing Applicants disclosed and claimed structure.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the

reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

2. Claim 27 stands rejected under 35 USC 103(a) as unpatentable over Parker et al. above taken with Dimmler et al. (US 6,787,440).

Applicants reiterate the comments made above with respect to Parker et al.

Dimmler discloses a ferroelectric FET structure having a completely different structure and working by a different principal of operation than either Dimmler et al. or Applicants disclosed and claimed invention. For example, Dimmler et al. discloses in one embodiment a **top buffer layer which is formed between the gate electrode and a top ferroelectric region** where the top ferroelectric region overlies a gate oxide layer which in turn overlies a bottom ferroelectric region (see Figure 6).

Even assuming *arguendo* proper motivation for combining the

teachings of Dimmler and Parker et al., such combination does not produce Applicants disclosed and claimed invention. The fact that Dimmler et al. teach a buffer layer having a high dielectric constant, as Examiner alleges, does not help Examiner in making out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claim 30 stands rejected under 35 USC 103(a) as unpatentable over Parker et al. above, in view of Tseng et al. (US 5,464,792).

Applicants reiterate the comments made above with respect to Parker et al.

Even assuming *arguendo*, a proper motivation for combining

the teachings of Parker et al. and Tseng et al., the fact that Tseng et al. teaches forming a buffer layer on a gate dielectric, forming a nitrogen source layer on the buffer layer, and then annealing the layers to drive nitrogen from the nitrogen source layer to the interface of the buffer layer and the gate dielectric (see Abstract), does not further help Examiner in producing Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

4. Claims 31-38 stand rejected under 35 USC 103(a) as unpatentable over Parker et al. above, in view of Nishikawa et al. (2004/0096692) or Dimmler et al. and Kim et al. (6,727,130) or Xiang (6,734,527).

Applicants reiterate the comments made above with respect to Parker et al. and Dimmler et al.

Even assuming *arguendo*, a proper motivation for combining the teachings of Parker et al. and Nishikawa et al., the fact that Nishikawa et al. teach:

"After an underlying layer, made of a single crystal metal material, has been formed on a semiconductor layer, part or all of the underlying layer is **changed into a metal oxide layer** by supplying oxygen thereto from above the underlying layer". (see Abstract); and at paragraph 0173 cited by Examiner: "In the structure shown in FIG. 12(a), a CeO.sub.2 layer 30, which is a **buffer layer made of a dielectric with a high dielectric constant, and a ferroelectric layer** 70 are formed on a clean and smooth surface of the Si substrate 17.";

Such teachings do not further help Examiner in producing Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

Even assuming *arguendo*, a proper motivation for combining the teachings of Parker et al. and Kim et al., the fact that Kim et al. teach that Al2O3, HfSiO2 can be employed in a gate insulating (dielectric) layer, as Examiner alleges, also does not further help Examiner in producing Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

Even assuming *arguendo*, a proper motivation for combining the teachings of Parker et al. and Xaing, the fact that Xaing teaches "CMOS devices including gate materials such as hafnium silicates, aluminum oxide and their application in MOS devices including NMOS and PMOS devices, as Examiner alleges, also does not further help Examiner in producing Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the

reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Based on the foregoing, Applicants respectfully request reconsideration of Applicants claims and submit that the Claims are in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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